**ANNA UNIVERSITY, CHENNAI**

**UNIVERSITY DEPARTMENTS**

**REGULATION – 2023**

**M.E APPLIED ELECTRONICS**

## VISION

To be recognized as a benchmark and trend setter in Electronics and Communication Engineering domain keeping in phase with rapidly changing technologies through effective partnership with reputed academic institutions, research organizations, industries and community.

## MISSION

- Create highly motivated, technologically competent human resource by imparting high quality technical education through flexible student centric updated curricula suited to students with diverse backgrounds
- Adopt best teaching and learning practices and establish state-of-the-art facilities to provide quality academic ambience for innovativeness, research and developmental activities
- Enhance collaborative activities with academic institutions and industries for evolving indigenous technological solutions to meet societal needs and nurture leadership and entrepreneurship qualities with ethical means.
- Facilitate adequate exposure to the students, faculty and staff through training in the state-of-the-art technologies, efficient administration, global outreach and benchmarking against referential institutions

PROGRESS THROUGH KNOWLEDGE

Attested

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**ANNA UNIVERSITY, CHENNAI**

**UNIVERSITY DEPARTMENTS**

**M.E. APPLIED ELECTRONICS (R-2023)**
**REGULATIONS – 2023**
**CHOICE BASED CREDIT SYSTEM**

## PROGRAMME EDUCATIONAL OBJECTIVES:

1. Graduates will expose technical problem solving skills with solid foundation in electronics, evolving advancements and remain committed for sustainable societal development.
2. Graduates will attain ability to excel in their future scope of career, research and role in engineering innovations by utilization of their electronics engineering foundation.
3. Graduates will develop skills for entrepreneurship, professional development and leadership in organizations by engaging in life-long learning process.

## PROGRAM OUTCOMES:

| PO# | GraduateAttribute | Programme Outcome |
|---|---|---|
| 1. | Research aptitude | An ability to independently carry out research/investigation and development work to solve practical problems. |
| 2. | Technical documentation | An ability to write and present a substantial technical report/document. |
| 3. | Technical competence | Students should be able to demonstrate a degree of mastery over Applied Electronics. |
| 4. | Engineering Design | An ability to apply various advanced tools and techniques of applied electronics to develop efficient hardware and software solutions. |
| 5. | The engineer and society | Apply technical knowledge towards the development of socially relevant products. |
| 6. | Environment and sustainability | Ensure development of eco-friendly indigenous products. |

## MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES WITH PROGRAMMEOUTCOMES:

A broad relation between the programme objective and the outcomes is given in the following table:

| PEOs | Programme Outcomes | | | | | |
|---|---|---|---|---|---|---|
| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
| I. | 3 | 2 | 3 | 2 | 3 | 3 |
| II. | 3 | 1 | 3 | 1 | 2 | 2 |
| III. | 3 | 1 | 2 | 1 | 1 | 2 |

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| | | COURSE NAME | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|---|---|
| Y | Semester 1 | Advanced Applied Mathematics | 3 | 3 | 3 | 3 | 2 | 2 |
| | | Embedded System Design | 1 | 1.5 | 2 | 2 | 1.75 | 2 |
| | | Statistical Signal Processing | 3 | 2 | 2.6 | 1.4 | 1 | 1 |
| | | Analog Integrated Circuit Design | 3 | 1.8 | 3 | 3 | 1 | |
| | | Research Methodology and IPR | | | | | | |
| | Semester 2 | Advanced Digital System Design | 2 | | 2.25 | 2.5 | 1.5 | |
| | | PCB Design and Fabrication | 2 | 1 | 2 | 2.75 | 2 | 3 |
| | | Digital CMOS VLSI Design | 1.75 | | 2.5 | 2.2 | 1 | |
| | | Professional Elective I | | | | | | |
| | | Professional Elective II | | | | | | |
| | | Signal Processing System Design Laboratory | 1.4 | 2.5 | 2.5 | 2.25 | 1 | |
| | | Idea to Product | | | | | | |
| YEA | Semester 3 | Professional Elective III | | | | | | |
| | | Professional Elective IV | | | | | | |
| | | Professional Elective V | | | | | | |
| | | Professional Elective VI | | | | | | |
| | | Project Work I | | | | | | |
| | Semester 4 | Project Work II | | | | | | |

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**M.E. APPLIED ELECTRONICS**

**REGULATIONS - 2023**

**CHOICE BASED CREDIT SYSTEM**

**CURRICULA AND SYLLABI**

**SEMESTER I**

| S. NO. | COURSE CODE | COURSE TITLE | CATEGORY | PERIODS PER WEEK | | | TOTAL CONTACT PERIODS | CREDITS |
|---|---|---|---|---|---|---|---|---|
| | | | | L | T | P | | |
| **THEORY** | | | | | | | | |
| 1. | MA3152 | Advanced Applied Mathematics | FC | 4 | 0 | 0 | 4 | 4 |
| 2. | RM3151 | Research Methodology and IPR | RMC | 2 | 1 | 0 | 3 | 3 |
| 3. | AP3101 | Embedded System Design | PCC | 3 | 0 | 4 | 7 | 5 |
| 4. | AP3102 | Statistical Signal Processing | PCC | 3 | 0 | 2 | 5 | 4 |
| 5. | AP3151 | Analog Integrated Circuit Design | PCC | 3 | 0 | 4 | 7 | 5 |
| | | | **TOTAL** | **15** | **1** | **10** | **26** | **21** |

**SEMESTER II**

| S. NO. | COURSE CODE | COURSE TITLE | CATEGORY | PERIODS PER WEEK | | | TOTAL CONTACT PERIODS | CREDITS |
|---|---|---|---|---|---|---|---|---|
| | | | | L | T | P | | |
| **THEORY** | | | | | | | | |
| 1. | AP3251 | Advanced Digital SystemDesign | PCC | 3 | 0 | 0 | 3 | 3 |
| 2. | AP3201 | PCB Design and Fabrication | PCC | 3 | 0 | 4 | 7 | 5 |
| 3. | VL3151 | Digital CMOS VLSI Design | PCC | 3 | 0 | 0 | 3 | 3 |
| 4. | | Professional Elective I | PEC | 3 | 0 | 0 | 3 | 3 |
| 5. | | Professional Elective II | PEC | 3 | 0 | 0 | 3 | 3 |
| **PRACTICALS** | | | | | | | | |
| 6. | AP3211 | Signal Processing System Design Laboratory | PCC | 0 | 0 | 4 | 4 | 2 |
| 7. | AP3212 | Idea to Product | EEC | 0 | 0 | 4 | 4 | 2 |
| | | | **TOTAL** | **15** | **0** | **12** | **27** | **21** |

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## SEMESTER III

| S. NO. | COURSE CODE | COURSE TITLE | CATE GORY | PERIODS PER WEEK | | | TOTAL CONTACT PERIODS | CREDITS |
|---|---|---|---|---|---|---|---|---|
| | | | | L | T | P | | |
| **THEORY** | | | | | | | | |
| 1. | | Professional Elective III | PEC | 3 | 0 | 0 | 3 | 3 |
| 2. | | Professional Elective IV | PEC | 3 | 0 | 0 | 3 | 3 |
| 3. | | Professional Elective V | PEC | 3 | 0 | 0 | 3 | 3 |
| 4. | | Professional Elective VI | PEC | 3 | 0 | 0 | 3 | 3 |
| **PRACTICALS** | | | | | | | | |
| 4. | AP3311 | Project Work I | EEC | 0 | 0 | 12 | 12 | 6 |
| | | | **TOTAL** | **12** | **0** | **12** | **24** | **18** |

## SEMESTER IV

| S. NO. | COURSE CODE | COURSE TITLE | CATE GORY | PERIODS PER WEEK | | | TOTAL CONTACT PERIODS | CREDITS |
|---|---|---|---|---|---|---|---|---|
| | | | | L | T | P | | |
| **PRACTICALS** | | | | | | | | |
| 1. | AP3411 | Project Work II | EEC | 0 | 0 | 24 | 24 | 12 |
| | | | **TOTAL** | **0** | **0** | **24** | **24** | **12** |

**TOTAL NO. OF CREDITS: 72**

## FOUNDATION COURSE (FC)

| S. NO. | COURSE CODE | COURSE TITLE | PERIODS PERWEEK | | | CREDITS | SEMESTER |
|---|---|---|---|---|---|---|---|
| | | | L | T | P | | |
| 1. | MA3152 | Advanced AppliedMathematics | 4 | 0 | 0 | 4 | I |

## PROFESSIONAL CORE COURSES (PCC)

| S. NO. | COURSE CODE | COURSE TITLE | PERIODS PER WEEK | | | CREDITS | SEMESTER |
|---|---|---|---|---|---|---|---|
| | | | L | T | P | | |
| 1. | AP3101 | Embedded System Design | 3 | 0 | 4 | 5 | I |
| 2. | AP3102 | Statistical Signal Processing | 3 | 0 | 2 | 4 | I |
| 3. | AP3151 | Analog Integrated CircuitDesign | 3 | 0 | 4 | 5 | I |
| 5. | AP3251 | Advanced Digital SystemDesign | 3 | 0 | 0 | 3 | II |
| 6. | AP3201 | PCB Design and Fabrication | 3 | 0 | 4 | 5 | II |



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| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7. | VL3151 | Digital CMOS VLSI Design | 3 | 0 | 0 | 3 | II |
| 8. | AP3211 | Signal Processing System Design Laboratory | 0 | 0 | 4 | 2 | II |

**RESEARCH METHODOLOGY AND IPR COURSES (RMC)**

| S. NO. | COURSE CODE | COURSE TITLE | PERIODS PER WEEK | | | CREDITS | SEMESTER |
|---|---|---|---|---|---|---|---|
| | | | L | T | P | | |
| 1. | RM3151 | Research Methodology and IPR | 2 | 1 | 0 | 3 | I |

**PROFESSIONAL ELECTIVE COURSES (PEC)**

| S. NO | COURSE CODE | COURSE TITLE | CATEGORY | PERIODS PER WEEK | | | CONTACT PERIODS | CREDITS |
|---|---|---|---|---|---|---|---|---|
| | | | | L | T | P | | |
| 1. | AP3001 | Digital Image Processing | PEC | 2 | 0 | 2 | 4 | 3 |
| 2. | AP3002 | DSP Integrated Circuits | PEC | 3 | 0 | 0 | 3 | 3 |
| 3. | AP3054 | Nonlinear Signal Processing | PEC | 3 | 0 | 0 | 3 | 3 |
| 4. | AP3003 | Advanced Digital Control Engineering | PEC | 3 | 0 | 0 | 3 | 3 |
| 5. | AP3004 | Programming Languages for Embedded Software | PEC | 2 | 1 | 0 | 3 | 3 |
| 6. | AP3005 | Advanced Computer Architecture Design | PEC | 3 | 0 | 0 | 3 | 3 |
| 7. | AP3006 | Design and Analysis of Computer Algorithms | PEC | 3 | 0 | 0 | 3 | 3 |
| 8. | AP3058 | Wireless Sensor Networks | PEC | 3 | 0 | 0 | 3 | 3 |
| 9. | AP3007 | IOT System Design and Security | PEC | 3 | 0 | 0 | 3 | 3 |
| 10. | AP3051 | Advanced Microprocessors and Microcontrollers | PEC | 3 | 0 | 0 | 3 | 3 |
| 11. | AP3052 | Electronics for Solar Power | PEC | 3 | 0 | 0 | 3 | 3 |
| 12. | AP3056 | Robotics and Intelligent Systems | PEC | 3 | 0 | 0 | 3 | 3 |
| 13. | AP3055 | RF Integrated Circuit Design | PEC | 3 | 0 | 0 | 3 | 3 |
| 14. | AP3057 | Signal Integrity for HighSpeed Design | PEC | 3 | 0 | 0 | 3 | 3 |
| 15. | AP3053 | EMI and EMC in System Design | PEC | 3 | 0 | 0 | 3 | 3 |
| 16. | AP3008 | Artificial Intelligence and Optimization Techniques | PEC | 3 | 0 | 0 | 3 | 3 |



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| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 17. | AP3009 | Nanoelectronics | PEC | 3 | 0 | 0 | 3 | 3 |
| 18. | VL3054 | MEMS and NEMS | PEC | 3 | 0 | 0 | 3 | 3 |
| 19. | VL3052 | Fundamentals of Spintronics and Quantum Computing | PEC | 3 | 0 | 0 | 3 | 3 |
| 20. | AP3010 | System Design using Hardware Description Languages | PEC | 2 | 0 | 2 | 4 | 3 |
| 21. | VL3055 | Neuromorphic Computing | PEC | 3 | 0 | 0 | 3 | 3 |
| 22. | VL3053 | Machine Learning in VLSI Design | PEC | 3 | 0 | 0 | 3 | 3 |

**EMPLOYABILITY ENHANCEMENT COURSES (EEC)**

| S.NO | COURSE CODE | COURSE TITLE | PERIODS PER WEEK | | | CREDITS | SEMESTER |
|---|---|---|---|---|---|---|---|
| | | | L | T | P | | |
| 1. | AP3212 | Idea to Product | 0 | 0 | 4 | 2 | II |
| 2. | AP3311 | Project Work I | 0 | 0 | 12 | 6 | III |
| 3. | AP3411 | Project Work II | 0 | 0 | 24 | 12 | IV |
| **TOTAL CREDITS** | | | | | | **20** | |

| | M.E APPLIED ELECTRONICS | | | | | |
|---|---|---|---|---|---|---|
| | SUBJECT AREA | CREDITS PER SEMESTER | | | | CREDITS TOTAL |
| | | I | II | III | IV | |
| 1. | FC | 4 | - | - | - | 4 |
| 2. | PCC | 14 | 13 | - | - | 27 |
| 3. | PEC | - | 6 | 12 | - | 18 |
| 4. | RMC | 3 | - | - | - | 3 |
| 5. | EEC | - | 2 | 6 | 12 | 20 |
| | **TOTAL CREDITS** | **21** | **21** | **18** | **12** | **72** |

PROGRESS THROUGH KNOWLEDGE

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**MA3152 ADVANCED APPLIED MATHEMATICS L T P C**
**4 0 0 4**

**UNIT I LINEAR ALGEBRA 12**

Vector spaces – norms – Inner Products – Eigenvalues using QR transformations – QR factorization - generalized eigenvectors – Canonical forms – singular value decomposition and applications - pseudo inverse – least square approximations --Toeplitz matrices and some applications.

**UNIT II ONE DIMENSIONAL RANDOM VARIABLES 12**

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

**UNIT III RANDOM PROCESSES 12**

Classification – Auto correlation - Cross correlation - Stationary random process – Markov process –- Markov chain - Poisson process – Gaussian process.

**UNIT IV LINEAR PROGRAMMING 12**

Formulation – Graphical solution – Simplex method – Two phase method - Transportation and Assignment Models

**UNIT V FOURIER TRANSFORM FOR PARTIAL DIFFERENTIAL EQUATIONS 12**

Fourier transforms: Definitions, properties-Transform of elementary functions, Dirac Delta functions – Convolution theorem – Parseval‘s identity – Solutions to partial differential equations: Heat equations, Wave equations, Laplace and Poisson‘s equations.

**TOTAL: 45+15=60 PERIODS**

**COURSE OUTCOMES:**

**At the end of the course, students will be able to**

**CO1** Apply the concepts of linear algebra to solve practical problems.
**CO2** Use the ideas of probability and random variables in solving engineering problems.
**CO3** Classify various random processes and solve problems involving stochastic processes.
**CO4** Formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems.
**CO5** Apply the Fourier transform methods of solving standard partial differential equations.

**REFERENCES:**


1. Andrews, L.C. and Philips.R.L., “Mathematical Techniques for engineering and scientists”, Printice Hall of India, New Delhi, 2006.
2. Bronson, R., “Matrix Operation”, Schaum‘s outline series, Tata McGrawHill, New York, 2011.
3. O‘Neil P.V., “Advanced Engineering Mathematics”, Cengage Learning, 8th Edition, India, 2017.
4. Oliver C. Ibe, “Fundamentals of Applied Probability and Random Processes”, Academic Press, Boston, 2014.
5. Sankara Rao, K., “Introduction to partial differential equations”, Prentice Hall of India, pvt, Ltd, 3rd Edition, New Delhi, 2010.
6. Taha H.A., “Operations Research: An introduction”, Ninth Edition, Pearson Education, Asia, 10th Edition, New Delhi, 2017.


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**CO-PO Mapping:**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 3 | 3 | 2 | 2 |
| **CO2** | 3 | 3 | 3 | 3 | 2 | 2 |
| **CO3** | 3 | 3 | 3 | 3 | 2 | 2 |
| **CO4** | 3 | 3 | 3 | 3 | 2 | 2 |
| **CO5** | 3 | 3 | 3 | 3 | 2 | 2 |
| **AVG** | 3 | 3 | 3 | 3 | 2 | 2 |

**RM3151 RESEARCH METHODOLOGY AND IPR L T P C**
**2 1 0 3**

**UNIT I RESEARCH PROBLEM FORMULATION 9**

Objectives of research, types of research, research process, approaches to research; conducting literature review- information sources, information retrieval, tools for identifying literature, Indexing and abstracting services, Citation indexes, summarizing the review, critical review, identifying research gap, conceptualizing and hypothesizing the research gap

**UNIT II RESEARCH DESIGN AND DATA COLLECTION 9**

Statistical design of experiments- types and principles; data types & classification; data collection - methods and tools

**UNIT III DATA ANALYSIS, INTERPRETATION AND REPORTING 9**

Sampling, sampling error, measures of central tendency and variation,; test of hypothesis- concepts; data presentation- types of tables and illustrations; guidelines for writing the abstract, introduction, methodology, results and discussion, conclusion sections of a manuscript; guidelines for writing thesis, research proposal; References – Styles and methods, Citation and listing system of documents; plagiarism, ethical considerations in research

**UNIT IV INTELLECTUAL PROPERTY RIGHTS 9**

Concept of IPR, types of IPR – Patent, Designs, Trademarks and Trade secrets, Geographical indications, Copy rights, applicability of these IPR; , IPR & biodiversity; IPR development process, role of WIPO and WTO in IPR establishments, common rules of IPR practices, types and features of IPR agreement, functions of UNESCO in IPR maintenance.

**UNIT V PATENTS 9**

Patents – objectives and benefits of patent, concept, features of patent, inventive steps, specifications, types of patent application; patenting process - patent filling, examination of patent, grant of patent, revocation; equitable assignments; Licenses, licensing of patents; patent agents, registration of patent agents.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**

Upon completion of the course, the student can

CO1: Describe different types of research; identify, review and define the research problem

CO2: Select suitable design of experiment s; describe types of data and the tools for collection of data

CO3: Explain the process of data analysis; interpret and present the result in suitable form

CO4: Explain about Intellectual property rights, types and procedures

CO5: Execute patent filing and licensing



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**REFERENCES:**


1. Cooper Donald R, Schindler Pamela S and Sharma JK, “Business Research Methods”, Tata McGraw Hill Education, 11e (2012).
2. Soumitro Banerjee, “Research methodology for natural sciences”, IISc Press, Kolkata, 2022,
3. Catherine J. Holland, “Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets”, Entrepreneur Press, 2007.
4. David Hunt, Long Nguyen, Matthew Rodgers, “Patent searching: tools & techniques”, Wiley, 2007.
5. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, “Professional Programme Intellectual Property Rights, Law and practice”, September 2013.


**AP3101 EMBEDDED SYSTEM DESIGN L T P C**

**3 0 4 5**

**UNIT I EMBEDDED COMPUTING PLATFORM – HARDWARE ASPECT 9**

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process - CPU: Programming input and output CPU performance – CPU power consumption- CPU buses – Memory devices – Input / Output devices – Component interfacing- Designing with microprocessor development and debugging.

**UNIT II EMBEDDED COMPUTING PLATFORM – SOFTWARE ASPECT 9**

Program design – Model of programs – Assembly and Linking – Basic compilation techniques – Program Optimization- Program validation and testing- Operating Systems – Priority based Scheduling- RMS and EDF –Context Switching- Inter Process Communication mechanisms – Evaluating operating system performance – Power optimization strategies for processes.

**UNIT III DISTRIBUTED EMBEDDED COMPUTING PLATFORM 9**

Multiprocessors- CPUs and Accelerators – Performance Analysis- Distributed Embedded Architecture – Networks for Embedded Systems: - $I^2C$ Bus, CAN Bus, SHARC Link Port-Ethernet, Myrinet – Network based design – Internet enabled systems-Network based system performance Analysis

**UNIT IV ARM PROCESSOR 9**

ARM Processor Fundamentals- ARM Cortex M3 Processor Architecture- MBED NXP LPC1768 – Pinout Details and Peripherals-ARM Assembly Language Instruction Set- Addressing Modes-Programming.

**UNIT V SYSTEM DESIGN – APPLICATION CASE STUDY 9**

Design Models, Quality Assurance, Design Example: Toy Train Controller, Digital Alarm Clock, Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Box.

**THEORY: 45 PERIODS**

**PRACTICAL EXERCISES: LAB: 60 PERIODS**

1. Push button, LED, LCD display and RTC interfacing with AVR RISC based microcontroller.



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2. AVR RISC based Microcontroller system design with Touch screen interfacing.
3. Motor (DC, stepper, servo) interfacing with AVR RISC based Microcontroller.
4. Interfacing sensors and RFID with AVR RISC based Microcontroller.
5. Design of RC5 remote control decoder with AVR RISC based Microcontroller.
6. Implementing I2C, SPI, CAN and UART protocols with ARM 7 processor.
7. Design and implementation of path tracking and obstacle avoidance Robot.
8. Design and implementation of self-balancing Robot.
9. Design and implementation of Robotic Arm manipulation with 6 DOF.
10. Design and implementation of Pick and Place robot.
11. Design and implementation of color and pattern guided material handling robot.
12. Design and implementation of human detection robot using PIR sensor.

**COURSE OUTCOMES:**

**CO1**: Ability to apply the hardware design concepts in developing an embedded system.

**CO2**: Ability to apply the software aspects embedded system design

**CO3**: Ability to apply networking principles in embedded devices using EDA tools, sensor, high power devices and motors effectively.

**CO4**: Ability to understand and use ARM processors in implementing embedded devices.

**CO5**: Ability to design suitable embedded systems for real world applications and demonstrate competence in working with different Robot Operating Systems(ROS).

**REFERENCES:**


1. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kaufman Publishers, 3rd Edition, 2012.
2. Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developer‘s Guide- Designing and Optimizing System Software", Elsevier/Morgan Kaufmann Publisher, 2008.
3. Ata Elahi, Trevor Arjeski, “ARM Assembly Language with Hardware Experiments”, Springer Publishing Company, 2015.
4. Jane.W.S. Liu, “Real-Time systems”, Pearson Education Asia, 2001.
5. C. M. Krishna and K. G. Shin, “Real-Time Systems”, McGraw-Hill, 1st Edition, Reprint on 2017.
6. Frank Vahid and Tony Givargis, “Embedded System Design: A Unified Hardware/Software Introduction”, John Wiley & Sons, 2006.


**TOTAL: 105 PERIODS**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 1 | | | | | |
| **CO2** | | 2 | | | 2 | |
| **CO3** | | | 3 | 2 | 1 | |
| **CO4** | 1 | | 2 | | 2 | 1 |
| **CO5** | | 1 | 1 | | 2 | 3 |

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| AP3102 | STATISTICAL SIGNAL PROCESSING | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 2 | 4 |

**UNIT I INTRODUCTION TO RANDOM SIGNAL PROCESSING 9**

Discrete Random Processes- Ensemble Averages, Stationary processes, Bias and Estimation, Autocovariance, Autocorrelation, Parseval's theorem, Wiener-Khintchine relation, White noise, Power Spectral Density, Spectral factorization, Filtering Random Processes.

**UNIT II SIGNAL MODELING 9**

ARMA (p,q), AR (p), MA (q) models, Forward Linear Prediction, Backward Linear Prediction: – Yule-Walker Method, Solution to Prony's normal equation, Levinson Durbin Algorithm.

**UNIT III SPECTRAL ESTIMATION 9**

Estimation of spectra from finite duration signals, Nonparametric methods - Periodogram, Modified periodogram, Bartlett, Welch and Blackman-Tukey methods, Parametric method, AR (p) spectral estimation and detection of Harmonic signals.

**UNIT IV LINEAR ESTIMATION 9**

Linear Minimum Mean-Square Error (LMMSE) Filtering: Wiener Hopf Equation, FIR Wiener filter, Noise Cancellation, Causal IIR Wiener filter, Non-causal IIR Wiener filter.

**UNIT V ADAPTIVE FILTERS 9**

FIR adaptive filters — adaptive filter based on steepest descent method- Widrow-Hopf LMS algorithm, Normalized LMS algorithm, Adaptive channel equalization, Adaptive echo cancellation, Adaptive noise cancellation, RLS adaptive algorithm.

**TOTAL: 45 PERIODS**

**PRACTICAL EXERCISES: LAB: 60 PERIODS**

Tools: any tool, MATLAB, SIMULINK, LABVIEW, any processor.

(Use only filtering and adaptive filtering, statistical analysis, feature extraction etc. Don't use machine learning, deep learning, AI, NN, CNN)

1. Simulate sum of three sinusoidal signals. Add white noise with various noise density and try to remove noise using appropriate filter. Try to find various statistical features and compare. Plot (i) I/P and O/P signal without noise in time domain and frequency domain (ii) I/P and O/P signal with noise in time domain and frequency domain

2. Try to record your voice in an ideal condition. Add noise with various noise density. Recover your signal using noise removal algorithm, i.e., using various filter. Try to find various statistical features and compare. Plot (i) I/P and O/P signal without noise in time domain and frequency domain (ii) I/P and O/P signal with noise in time domain and frequency domain

3. Try to record all your (Classmates) voices. Try to separate each of the voice from mixed of all voices. Assumptions you can made

4. Try to say or sing the same line, Pick the signal(s) in the ideal environment, Pick the signal(s) in the noisy environment (known noise or unknown noise(noise can be added by picking the signal when all the fans in the room are running))



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5. Take any song of your choice. Try to separate each of the component in that song. (Music instruments, voice, etc). If possible add noise and try to recover the original song

6. Pick different bird sounds (separately and mixed together) (with and without noise) (if possible in our campus). Try to label it .

7. Do the same as in question 4 for different animals

8. Try to do the same in question 2, for different age groups (ex: age 4 to age 80)

**COURSE OUTCOMES:**

**CO1**: Ability to analyze discrete time random processes.
**CO2**: Ability to obtain models for prediction and Estimation.
**CO3**: Ability to analyze non-parametric methods and parametric methods for spectral estimation.
**CO4**: Ability to design different MMSE filters and adaptive filters for different applications.
**CO5**: Ability to develop a system for real time applications using any tool..

**REFERENCES:**


1. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley andSons, Inc, Singapore, 2002.
2. Dimitris G. Manolakis and Vinay K .Ingle, "Applied Digital Signal Processing", Cambridge University Press, 2011.
3. M. Kay's, "Fundamentals of Statistical Signal Processing: Estimation Theory (Vol 1), Detection Theory (Vol 2)", Prentice Hall Signal Processing Series, 1993.
4. Kailath, Sayed and Hassibi, "Linear Estimation, Information and Sciences Series", Prentice Hall, 1st Edition, 2000.


| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 2 | 1 | | |
| **CO2** | 3 | 2 | 2 | 1 | | |
| **CO3** | 3 | 2 | 3 | 1 | | |
| **CO4** | 3 | 2 | 3 | 2 | 1 | 1 |
| **CO5** | 3 | 2 | 3 | 2 | 1 | 1 |

**AP3151 ANALOG INTEGRATED CIRCUIT DESIGN L T P C**
**3 0 4 5**

**UNIT I SINGLE STAGE AMPLIFIERS 9**

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower differential with active load, Cascode and folded Cascode configurations with active load, Design of differential and Cascode amplifiers – to meet specified SR, gain, BW, ICMR and power dissipation, voltage swing, High gain amplifier, structures.



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**UNIT II HIGH FREQUENCY AND NOISE CHARACTERISTICS OFAMPLIFIERS 9**

Miller effect, association of poles with nodes, frequency response of CS, CG and sourcefollower, Cascode and differential pair stages, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

**UNIT III NEGATIVE FEEDBACK AMPLIFIERS AND OPERATIONAL AMPLIFIERS 9**

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, One-stage OpAmps, Two-stage OpAmps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in OpAmps.

**UNIT IV STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE OPERATIONAL AMPLIFIER 9**

Analysis of two stage OpAmp – two stage OpAmp single stage CMOS CS as second stage and using Cascode second stage, multiple systems, Phase Margin, Frequency Compensation, and Compensation of two stage OpAmps, Slewing in two stage OpAmps, Other compensation techniques.

**UNIT V VOLTAGE AND CURRENT REFERENCES 9**

Current sinks and sources, Current mirrors, Wilson current source, Widlar current source, Cascode current source, Design of high swing Cascode sink, current amplifiers, Supply independent biasing, temperature independent references, PTAT and CTAT current generation, Constant-Gm Biasing.

**TOTAL: 45 PERIODS**

**PRACTICAL EXERCISES:**

1. Extraction of process parameters of CMOS process Transistors
    a. Plot ID vs. VGS at different drain voltages for nMOS, PMOS.
    b. Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.
    c. Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.
    d. Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
2. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.
    a. Calculate input bias voltage for a given bias current.
    b. Use spice and obtain the bias current. Compare with the theoretical value
    c. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in spice, considering load capacitance.
    d. Plot step response of the amplifier with a specific input pulse amplitude. Derive time constant of the output and compare it with the time constant resulted from -3dB BW.
    e. Use spice to determine input voltage range of the amplifier.
3. Realize layout and perform post layout simulation of the CS amplifier realized in Ex.No.2
4. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter
    a. Perform DC analysis and determine input common mode range and compare with the theoretical values.
    b. Perform time domain simulation and verify low frequency gain.
    c. Perform AC analysis and verify low-frequency voltage gain and unity gain BW (fu)



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5. Stability Analysis of Two stage OpAmp
    a. Perform DC analysis and determine input common mode range and compare with the theoretical values.
    b. Perform time domain simulation and verify low frequency gain.
    c. Perform AC analysis and verify low-frequency voltage gain and unity gain BW (fu)

**COURSE OUTCOMES:**

**CO1**: Ability to design amplifiers to meet user specifications
**CO2**: Ability to analyse the frequency and noise performance of amplifiers
**CO3**: Ability to design and analyse negative feedback amplifiers and opAmps
**CO4**: Ability to analyse stability aspects of two stage opAmps
**CO5**: Ability to design and use current mirrors, current sources using MOS devices

**REFERENCES:**


1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2nd Edition, 2016.
2. Willey M.C. Sansen, "Analog Design Essentials", Springer, March 2007.
3. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley & sons,Inc.,2003.
4. Phillip E.Allen, Douglas R.Holberg, "CMOS Analog Circuit Design", Oxford University Press, 3rd October 2013.
5. Recorded lecture available at http://www.ee.iitm.ac.in/~ani/ee5390/index.html
6. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley IEEE Press, 4th Edition,August 2019.


**Articulation Matrix:**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 3 | 3 | 1 | |
| **CO2** | 3 | 3 | 3 | 3 | 1 | |
| **CO3** | 3 | 1 | 3 | 3 | 1 | |
| **CO4** | 3 | 1 | 3 | 3 | 1 | |
| **CO5** | 3 | 1 | 3 | 3 | 1 | |

**AP3251 ADVANCED DIGITAL SYSTEM DESIGN** **L T P C**

**3 0 0 3**

**UNIT I SEQUENTIAL CIRCUIT DESIGN 9**

Analysis of clocked synchronous sequential circuits and modelling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits - design of iterative circuits-ASM chart and realization using ASM.

**UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9**

Analysis of asynchronous sequential circuit — flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards — mixed operating mode asynchronous circuits — designing vending machine controller.

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**UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9**

Fault table method-path sensitization method – Boolean difference method - D algorithm – Kohavi algorithm — Tolerance techniques — The compact algorithm — Fault in PLA — Test generation-DFT schemes – Built in self-test.

**UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9**

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Designing ROM with PLA – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000.

**UNIT V SYSTEM DESIGN USING VERILOG 9**

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modelling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers — counters — sequential machine — serial adder — Multiplier- Divider — Design ofsimple microprocessor.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES:**

**CO1**: Ability to analyse and design synchronous sequential circuits.
**CO2**: Ability to analyse hazards and design asynchronous sequential circuits.
**CO3**: Ability to apply the testing procedure for combinational circuit and PLA.
**CO4**: Able to design PLD and ROM.
**CO5**: Ability to design and use programming tools for implementing digital circuits.

**REFERENCES:**


1. Charles H.Roth Jr, “Fundamentals of Logic Design”, Thomson Learning, 7th Edition, 2013.
2. M.D.Ciletti, “Modeling, Synthesis and Rapid Prototyping with the Verilog HDL”, Prentice Hall, 1997.
3. M.G.Arnold, “Verilog Digital – Computer Design”, Prentice Hall (PTR), 1999.
4. Nripendra N Biswas, “Logic Design Theory”, Prentice Hall of India, 2001.
5. Parag K. Lala, “Fault Tolerant and Fault Testable Hardware Design”, B S Publications, 2020.
6. Parag K. Lala, “Digital system Design using PLD”, B S Publications, Reprint 2015.
7. S. Palnitkar, “Verilog HDL – A Guide to Digital Design and Synthesis”, Pearson, 2003.


| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | | | 2 | | | |
| **CO2** | | | 2 | | | |
| **CO3** | 2 | | 2 | 3 | 1 | |
| **CO4** | | | 3 | | 2 | |
| **CO5** | | | | 2 | | |

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**AP3201** **PCB DESIGN AND FABRICATION** **L T P C**
**3 0 4 5**

**UNIT I BASICS OF PCB DESIGN, TOOLS & INDUSTRY STANDARDS 9**

Printed Circuit Board Fabrication- PCB cores and layer stack-up. PCB fabrication process- Photolithography and chemical etching, Mechanical milling and Layer registration. Function of the Layout in the PCB Design Process. Design Files Created by Layout - Layout format files, Postprocess (Gerber) files, PCB assembly layers and files. Introduction to the Standards Organizations, Classes and Types of PCBs, Introduction to Standard Fabrication Allowances, PCB Dimensions and Tolerances, Copper Trace and Etching Tolerances, Standard Hole Dimensions, Soldermask Tolerance.

**UNIT II PCB DESIGN FLOW USING CAD TOOL 9**

Overview of Computer-Aided Design. Setting up the user account, Starting a new project, Schematic Entry, Placing and wiring (connecting) the parts, Converting Schematic to Layout, Layout Environment and Tool Set, Designing the PCB with Layout – Setting constraints, Placing the parts, Auto routing and the Manual routing, Performing a design rule check, Making a board outline, Post processing the board design for manufacturing, Submitting Gerber files and requesting a quote, Annotating the layer types and stack-up, Receipt inspection and testing, Nonstandard Gerber files.

**UNIT III DESIGN CONSTRAINTS FOR MANUFACTURING 9**

PCB Assembly and Soldering Processes- Component Placement and Orientation Guide, Component Spacing for Through-hole Devices (THDs). Component Spacing for Surface Mounted Devices (SMDs), Mixed THD and SMD Spacing Requirements. Footprint and Pad stack Design for PCB Manufacturability- Land Patterns for SMDs- Land Patterns for THDs, Pad stack design, Hole-to-lead ratio, PTH land dimension (annular ring width), Clearance between plane layers and PTHs Solder mask and solder paste dimensions.

**UNIT IV PCB DESIGN FOR SIGNAL INTEGRITY 9**

Signal Integrity Overview, Differential Traces and Impedance, Power Systems, Circuit Design Issues Not Related to PCB Layout, Issues Related to PCB Layout – surge, transient, crosstalk, ESD, Ground Planes and Ground Bounce, PCB Electrical Characteristics, PCB Routing Topics.

**UNIT V EMERGING PCB FABRICATION PROCESSES 9**

Additive manufacturing – Fundamentals, classification, advantages and standards. Stereo lithography (SL), Three Dimensional Printing - FDM, Materials and Applications, Voltera-V-one PCB double side Printer, Bot Factory- SV2-multi layer PCB printer, LPKF circuit board plotter and LDS Prototyping, Subtractive manufacturing – Laser technology (IPG and Raycus).

**TOTAL: 45 PERIODS**

**PRACTICAL EXERCISES:** **LAB: 60 PERIODS**

1. Schematic capture using EDA tool.
2. Prepare PCB design layout and generate Gerber files and other files formats.
3. Design and fabrication of single layer PCB using traditional method.
4. PTH and via drilling in PCB by manual and automated (Bantam tools) methods.
5. Mechanical registration and riveting of PTH and via.
6. Design and fabrication of double layer PCB using laser technology.
7. Design and fabrication of PCB using Bantam tools (milling process).



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8. Design and fabrication of PCB using Voltera V-one machine.
9. Design and fabrication of PCB using Bot Factory – SV2 multilayer PCB printing.
10. SMD placing on PCB using pick and place machine.
11. PCB assembly of SMD using reflow soldering with temperature profiling of reflow oven.
12. PCB assembly of THD using manual and robotic soldering.
13. PCB assembly of THD using Wave soldering and its temperature profiling.
14. Design and fabricate PCB for AVR RISC based microcontroller development board.
15. Perform PCB assembly in the microcontroller development board.
16. Optical inspection and Verification of the microcontroller development board.
17. Conductive emission and Radiative emission test for PCB.

**TOTAL: 105 PERIODS**

**COURSE OUTCOMES**

**At the end of the course students will be able to:**

**CO1**: To understand the basics, industry standards organizations related to the design and fabrication of PCBs by using EDA tools.

**CO2**: Leads new users of the software through a very simple design.

**CO3**: To know and guide in designing plated through-holes, surface-mount lands, and Layout footprints in general while designing a schematic diagram.

**CO4**: To know to construct Capture parts using the Capture Library Manager and Part Editorand the PSpice Model Editor.

**CO5**: To understand and to fabricate PCBs by different fabrication methods.

**REFERENCES:**


1. Kraig Mitzner, “Complete PCB Design Using OrCAD Capture and Layout”, Newness, 1st Edition, 2009.
2. Simon Monk, “Make your Own PCBs with EAGLE: From Schematic Design to Finished Boards”, McGraw-Hill Education TAB; 2nd Edition, 2017.
3. Douglas Brooks, “Signal Integrity Issues and Printed Circuit Board Design”, Prentice Hall PTR, 2012.
4. Lee W. Ritchey, John Zasio, Kella J. Knack, “Right the First Time: a Practical Handbookon High Speed PCB and System Design”, Speeding Edge, 2003.


| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 2 | | | | | |
| **CO2** | | | 3 | | | |
| **CO3** | | | 2 | | | |
| **CO4** | | | 2 | 3 | | |
| **CO5** | | 1 | 1 | 3 | 2 | 3 |

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**VL3151** **DIGITAL CMOS VLSI DESIGN** **L T P C**

**3 0 0 3**

**UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 12**

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter-Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters, Stick diagram and Layout diagrams.

**UNIT II COMBINATIONAL LOGIC CIRCUITS 9**

Static CMOS design, Different styles of logic circuits, Logical effort of complex gates, Static and Dynamic properties of complex gates, Interconnect Delay, Dynamic Logic Gates.

**UNIT III SEQUENTIAL LOGIC CIRCUITS 9**

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Nonbistable Sequential Circuits.

**UNIT IV ARITHMETIC BUILDING BLOCKS 9**

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs

**UNIT V MEMORY ARCHITECTURES 6**

Memory Architectures and Memory control circuits: Read-Only Memories, ROM cells, Read- write memories (RAM), dynamic memory design, 6 transistor SRAM cell, Sense amplifiers.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES:**

**CO1**: To be able to use mathematical methods and circuit analysis models in analysis of CMOS digital circuits.

**CO2**: To be able to create models of moderately sized static CMOS combinational circuits that realize specified digital functions and to optimize combinational circuit delay using RC delay models and logical effort.

**CO3**: To be able to design sequential logic at the transistor level and compare the tradeoffs of sequencing elements including flip-flops, transparent latches.

**CO4**: To be able to learn design methodology of arithmetic building blocks.

**CO5**: To be able to design functional units including ROM and SRAM.

PROGRESS THROUGH KNOWLEDGE

**REFERENCES:**

1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, “Digital Integrated Circuits: A Design Perspective”, Prentice Hall of India”, 2nd Edition, May 2016.
2. N.Weste, K. Eshraghian, “Principles of CMOS VLSI Design”, Addison Wesley, 2nd Edition, 1993.
3. M J Smith, “Application Specific Integrated Circuits”, Addison Wesley, January 2002.
4. Sung-Mo Kang & Yusuf Leblebici, “CMOS Digital Integrated Circuits Analysis and Design”, McGraw-Hill, 2002.

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**CO-PO MAPPING:**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 1 | | | 1 | 1 | |
| **CO2** | 1 | | 2 | 1 | 1 | |
| **CO3** | 1 | | | 1 | 1 | |
| **CO4** | 1 | | 2 | 1 | 1 | |
| **CO5** | 1 | | | 1 | 1 | |
| **Avg.** | 1 | | 2 | 1 | 1 | |

**AP3211 SIGNAL PROCESSING SYSTEM DESIGN LABORATORY L T P C**
**0 0 4 2**

**LIST OF EXPERIMENTS:**

1) HDL realization and timing analysis of
   i. Combinational circuits namely 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder.
   ii. Sequential circuits namely D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters.
2) FPGA implementation of PCI Bus & arbiter.
3) Realization of UART/ USART implementation in HDL and design validationusing test vector generation.
4) FPGA realization of single port SRAM and capturing the signal in DSO.
5) Back annotation and timing analysis of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.
6) Realization of Discrete Fourier transform/Fast Fourier Transform algorithm in HDL and observing the spectrum in simulation.
7) Design and implement FIR and IIR filters.
8) Design and implement adaptive filters.

**TOTAL: 60 PERIODS**

**COURSE OUTCOMES:**

**At the end of the course students will be able to:**

**CO1**:Ability to Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.
**CO2**: Ability to Validate the design in FPGA starting from design entry to back annotation.
**CO3**: Ability to Use EDA tools like Cadence/Mentor Graphics/ Xilinx/Altera Quartus.
**CO4**: Ability to Develop Fourier Transform algorithm in HDL.
**CO5**: Ability to Implement filters using HDL.

**Articulation Matrix:**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 1 | | | 2 | 1 | |
| **CO2** | 2 | 2 | 2 | 2 | 1 | |
| **CO3** | 1 | | | 2 | 1 | |
| **CO4** | 3 | 3 | 3 | 3 | 1 | |
| **CO5** | 3 | 3 | 3 | 3 | 1 | |



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**AP3001** **DIGITAL IMAGE PROCESSING** **L T P C**
**2 0 2 3**

**UNIT I DIGITAL IMAGE FUNDAMENTALS 12**

Image Acquisition, Elements of visual perception, Image sampling, Quantization, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform, Simulation of basic image processing operations using mathematical tools and image transforms.

**UNIT II IMAGE ENHANCEMENT AND RESTORATION 12**

Image Enhancement in the Spatial Domain - Basic Gray Level Transformations, Histogram Processing, Smoothing Spatial and Sharpening Spatial Filters, Enhancement in the Frequency Domain- Homomorphic Filtering, Color image processing, Image restoration - Model of the Image Restoration Process. Noise Models. Periodic Noise Reduction by Frequency Domain Filtering. Inverse Filtering. Minimum Mean Square Error (Wiener) Filtering. Geometric Transformations. Simulation of enhancement techniques and Wiener filtering.

**UNIT III IMAGE SEGMENTATION AND MORPHOLOGY 12**

Image segmentation - Edge detection, Edge linking, Thresholding, Region growing, Region splitting and Merging, Morphological Image Processing - Basics, SE, Erosion, Dilation, Opening, Closing, Hit-or-Miss Transform, Boundary Detection, Hole filling, Connected components, convex hull, thinning, thickening, skeletons, pruning, Geodesic Dilation, Erosion, Reconstruction by dilation and erosion. Simulation of Canny edge detection, Otsu Thresholding and Morphological operations.

**UNIT IV IMAGE COMPRESSION 12**

Lossless and Lossy compression: Variable length coding, LZW, transform coding, JPEG and MPEG compression standards. Simulation of coding techniques.

**UNIT V FEATURE EXTRACTION AND PATTERN CLASSIFICATION 12**

Boundary Representation - Chain codes, Boundary Descriptors, Region Descriptors, Scale-invariant Feature Transform Features, Speed-up Robust Features, Principal Components.Object Recognition - Patterns and pattern classes, Prototype Matching by minimum distance classifier, Matching by correlation, Optimum Bayes Statistical Classifiers. Case study on image segmentation and classification for real-world applications.

**TOTAL: 60 PERIODS**

**COURSE OUTCOMES:**

- **CO1**: Ability to analyze image acquisition and apply transforms specific to applications.
- **CO2**: Ability to apply enhancement in both spatial and frequency domain and implement algorithms to restore degraded images.
- **CO3**: Ability to develop and apply algorithms to extract objects of interest in images
- **CO4**: Ability to apply image compression algorithms
- **CO5**: Ability to interpret extracted object and its use in recognition.

**REFERENCES:**


1. Rafael C. Gonzalez, Richard E. Woods, "Digital Image Processing"‘, Pearson, Education, Inc., 4th Edition, 2018.
2. Anil K. Jain, “Fundamentals of Digital Image Processing”, Prentice Hall of India, 2002.
3. William K. Pratt, "Digital Image Processing", John Wiley, New York, 2002.
4. William K. Pratt, “Digital Image Processing”, John Wiley, New York, 2007.
5. D.E. Dudgeon and RM. Mersereau, "Multidimensional Digital Signal Processing", Prentice




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Hall Professional Technical Reference, 1990.
6. Milan Sonka et al, “Image Processing, Analysis and Machine Vision”, Brookes/Cole, VikasPublishing House, 2nd Edition, 1999;
7. Alan C. Bovik, "Handbook of image and Video Processing ", Elsevier Academic press, 2005.
8. S.Sridhar, "Digital Image Processing" Oxford University press, Edition 2011.

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 1 | | | | | |
| **CO2** | 1 | | 3 | 2 | | |
| **CO3** | 1 | | 3 | 2 | | |
| **CO4** | 1 | | 3 | 2 | | |
| **CO5** | 1 | | 3 | 2 | 1 | |

**AP3002 DSP INTEGRATED CIRCUITS L T P C**
**3 0 0 3**

**UNIT I INTRODUCTION TO DSP INTEGRATED CIRCUITS 9**

Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, FFT-The Fast Fourier Transform Algorithm, Discrete cosine transforms, Image coding, Adaptive DSP algorithms, Standard digital signal processors, Application specific IC"s for DSP, DSP system design, Integrated circuit design.

**UNIT II DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 12**

FIR filters, FIR filter structures, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Signal flow graphs, Filter structures, Mapping of analog filter structures, Finite word length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise. Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters.

**UNIT III DSP ARCHITECTURES 9**

DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture. TMS320C54x and TMS320C6x architecture, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures.

**UNIT IV SYNTHESIS OF DSP ARCHITECTURES & ARITHMETIC UNIT 9**

Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

Arithmetic Unit : Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator.

**UNIT V CASE STUDY-INTEGRATED CIRCUIT DESIGN 6**

Layout of VLSI circuits, Layout Styles, Case Study: FFT processor, DCT processor and Interpolator.

**TOTAL: 45 PERIODS**

Attested

**COURSE OUTCOMES:**

**CO1**: Ability to analyze and design fundamental signal processing algorithms and systems.



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**CO2**: Adequacy to design and analyze digital filter concepts and structures.
**CO3**: Equipped to design general purpose digital signal processors.
**CO4**: Ability to use various implementation strategies for signal processing algorithms.
**CO5**: Equipped to design signal processing VLSI systems.

**REFERENCES:**


1. Lars Wanhammar, "DSP Integrated Circuits", Academic press, New York, 1999.
2. John J. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Pearson Education, 4th Edition 2007.
3. Avtar Singh, S.Srinivasan, "Digital Signal Processing Implementations: Using DSP Microprocessors (with examples from TMS320C54XX), Thomson Publications, 2004.
4. Rulph Chassaing, Donald Reay, "Digital Signal Processing and Applications with the TMS320C6713 and TMS320C6416 DSK", John Wiley & Sons, 2008.
5. B.Venkatramani, M.Bhaskar, "Digital Signal Processors", Tata McGraw-Hill, 2002.
6. Keshab K.Parhi, "VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.
7. Emmanuel C. Ifeachor, Barrie W. Jervis, "Digital signal processing – A practical approach", Tata McGraw-Hill, 2006.


| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 1 | | 3 | | | |
| **CO2** | 2 | | 3 | | | |
| **CO3** | 2 | | 3 | | | |
| **CO4** | 2 | | 3 | | | |
| **CO5** | 2 | | 3 | | | |

**AP3054 NONLINEAR SIGNAL PROCESSING L T P C**
**3 0 0 3**

**UNIT I INTRODUCTION TO NONLINEAR FILTERS AND STATISTICAL PRELIMINARIES 9**

Nonlinear filters – measure of robustness – M estimators – L estimators – R estimators – order statistics – median filter and their characteristics – impulsive noise filtering by median filters – Recursive and weighted median filters – stock filters.

**UNIT II NON LINEAR DIGITAL SIGNAL PROCESSING BASED ON ORDER STATISTICS 9**

Time ordered nonlinear filters – rank ordered nonlinear filters – max/median filtering – median hybrid filters — characteristics of ranked order filters — L filters — M filters — R filters — comparison.

**UNIT III ADAPTIVE NONLINEAR AND POLYNOMIAL FILTERS 9**

Definition of polynomial filters – Wiener filters – robust estimation of scale – Adaptive filter based on local statistics – Decision directed filters – Adaptive L filters – Comparison of adaptive nonlinear filters – Neural networks for nonlinear filter

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**UNIT IV ALGORITHMS AND ARCHITECTURES 9**

Sorting and selection algorithm – running median algorithm – fast structures for median and order statistics filtering – systolic array implementation – Wave front array implementation – quadratic digital filters implementation

**UNIT V APPLICATIONS OF NONLINEAR FILTERS 9**

Power spectrum analysis – Morphological image processing – nonlinear edge detection impulse noise rejection in image and bio signals – two component image filtering – speech processing

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**

**CO1**: Ability to evaluate the characteristics of nonlinear filters

**CO2**: Ability to design and implement rank order filters.

**CO3**: Ability to develop polynomial filters.

**CO4**: Ability to design architectures for nonlinear filters.

**CO5**: Ability to implement nonlinear filters for different types of signals.

**REFERENCES:**


1. Ioannis Pitas, Anastarios. N.Venetsanopoulos, “Nonlinear Digital filters — Principles andApplications”, Kluwer Academic Publishers, 1990.
2. Jaakko Astola, P Kuosmanen, “Fundamentals of Nonlinear Digital Filtering”, CRC Press LLC, 1st Edition 2020.
3. Gonzalo R. Arce, “Nonlinear Signal Processing – A Statistical Approach”, Wiley Publishers,2005
4. Wing Kuen Ling, “Nonlinear Digital Filters: Analysis and Applications”, Elsevier Science &Tech. 2007.


| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | | | 2 | 2 | | |
| **CO2** | | | 3 | 2 | | |
| **CO3** | | | 3 | 3 | | |
| **CO4** | 1 | | 3 | 3 | 1 | 1 |
| **CO5** | 1 | | 3 | 3 | 1 | 1 |

**AP3003 ADVANCED DIGITAL CONTROL ENGINEERING L T P C**

**3 0 0 3**

**UNIT I PRINCIPLES OF CONTROLLERS 9**

Review of frequency and time response analysis and specifications of control systems, need for controllers, continues time compensations, continues time PI, PD, PID controllers, digital PID controllers.

**UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL 9**

Sampling, time and frequency domain description, aliasing, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

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**UNIT III MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM 9**

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state variable concepts, first companion, second companion, Jordan canonical models, discrete state variable models, elementary principles.

**UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9**

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

**UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9**

Algorithm development of PID control algorithms, software implementation, implementation using microprocessors and microcontrollers, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES:**

**CO1**: Ability to understand the concepts of discrete system science related mathematics and principlesof controllers.

**CO2**: Ability to explain the discrete system, component or process to meet desired needs for signal processing in digital control systems.

**CO3**: Ability to understand the Z-transform to process time sequences and solve difference equations to characterize the stability, frequency response, transient time response and steady-state error of a digital control system.

**CO4**: Ability to design digital controllers in the z-domain and by approximation of S-domain design to solve discrete control engineering problems.

**CO5**: Ability to understand the techniques, tools and skills related to discrete signals, computer science and modern discrete control engineering in modern engineering practice.

**REFERENCES:**


1. M.Gopal, “Digital Control and Static Variable Methods”, Tata McGraw Hill, New Delhi, 1997.
2. John J. D'Azzo, “Constantive Houpios, “Linear Control System Analysis and Design”, McGraw-Hill, 1995.
3. Kenneth J. Ayala, “The 8051 Microcontroller- Architecture, Programming and Applications”, Penram International, 2nd Edition, 2005.


PROGRESS THROUGH KNOWLEDGE

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| **CO1** | 1 | | | | 1 | |
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**AP3004 PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE L T P C**
**2 1 0 3**

**UNIT I EMBEDDED 'C' 9**

Programming Bitwise operations, Dynamic memory allocation, OS services Linked list, stack and queue, Sparse matrices, Binary tree. Interrupt handling in C, Code optimization issues. Writing LCD drives, LED drivers, Drivers for serial port communication. Embedded Software Development Cycle & Methods (Waterfall, Agile)

**UNIT II OBJECT ORIENTED PROGRAMMING 9**

Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism

**UNIT III CPP PROGRAMMING 9**

'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation

**UNIT IV OVERLOADING AND INHERITANCE 9**

Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions,

**UNIT V TEMPLATES 9**

Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions. **Scripting Languages:** Overview of Scripting Languages — PERL, CGI, VB Script, Java Script. PERL

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES:**

**CO1:** Ability to write an embedded C application of moderate complexity**.**
**CO2:** Ability to develop and analyze algorithms in C++.
**CO3:** Ability to differentiate interpreted languages from compiled languages.
**CO4:** Ability to differentiate the concepts of overloading and inheritance.
**CO5**: Ability to develop templates for different scripting languages.

**REFERENCES:**


1. Michael J. Pont, "Embedded C", Pearson Education, 2nd Edition, 2008.
2. Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition 2011.
3. A. Michael Berman, "Data structures via C++", Oxford University Press, 2002.
4. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999.
5. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey &Sons, 8th Edition 2008.


| COs | PROGRAMME OUTCOMES | | | | | |
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**AP3005 ADVANCED COMPUTER ARCHITECTURE DESIGN L T P C**
**3 0 0 3**

**UNIT I THEORY OF PARALLELIS 9**

Parallel computer models - the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties- Conditions of parallelism.

**UNIT II PARTITIONING AND SCHEDULING 9**

Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance - performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

**UNIT III HARDWARE TECHNOLOGIES 9**

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory — Bus Arbitration, cache memory organisations, shared memory organisations, sequential and weak consistency models.

**UNIT IV PIPELINING, SUPERSCALAR, PARALLEL AND SCALABLE ARCHITECTURE 9**

Linear and Non-Linear Pipeline processor – Instruction and Arithmetic Pipeline Design – Superscalar and Superpipeline Design – Multiprocessor Interconnects – Cache Coherence and Synchronization mechanism – Message Passing Mechanism – Flow Control Strategies – Multicast Routing Strategies

**UNIT V MULTIVECTOR AND SIMD COMPUTERS 9**

Vector processing Principles – Compound Vector Processing – SIMD Computer Organisation –Synchronized MIMD machine – Latency Hiding Technique – Multithreading –Scalable and Multithreaded Architectures – Data Flow and Hybrid Architectures - Parallel models, Languages and compilers, Parallel program development and environments.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES:**

**CO1**: Able to build up on advanced concepts of parallel architecture.
**CO2**: Able to design parallel architectures for improved performance
**CO3**: Ability to apply memory hierarchy for multiprocessor system.
**CO4**: Able to analyze the design structures of pipelined systems.
**CO5**: Able to analyze and design multiprocessor systems.

**REFERENCES**


1. Kai Hwang, "Advanced Computer Architecture", McGraw Hill International, 2003.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, “Advanced Computer Architecture — A Design Space Approach”, Pearson Education, 2003.
3. John P.Shen, “Modern Processor Design Fundamentals of Super Scalar Processors”, Tata McGraw Hill, 2003.




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4. Kai Hwang, “Scalable parallel computing”, Tata McGraw Hill 1998.
5. William Stallings, “Computer Organization and Architecture”, Macmillan Publishing Company, 9th Edition 2013.
6. M.J. Quinn, “Designing Efficient Algorithms for Parallel Computers”, McGraw Hill International, 1994.
7. Barry, Wilkinson, Michael, Allen “Parallel Programming”, Pearson Education Asia, 2nd Edition, 2005.
8. Harry F. Jordan Gita Alaghband, “Fundamentals of parallel Processing”, Pearson Education, 1st Edition 2003.
9. Richard Y.Kain, “Advanced Computer Architecture — A Systems Design Approach”, PHI, 2003.

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| **CO1** | 2 | | 2 | 3 | | |
| **CO2** | 1 | | 2 | | | |
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**AP3006 DESIGN AND ANALYSIS OF COMPUTER ALGORITHMS L T P C**
**3 0 0 3**

**UNIT I INTRODUCTION 9**

Introduction to Design and Analysis of Algorithms – Good Programming Practice – Problems to Programs – Algorithms and their Complexity – Models of Computation – Turing Machine.

**UNIT II DATA STRUCTURES 9**

Introduction to Data Structures — Linear and Non-linear Data Structures — Lists — Stack — Queue — Graph — Tree — Data Structure Operations - Shortest Path Algorithms — MinimalSpanning Tree Construction.

**UNIT III ALGORITHMS ANALYSIS AND DESIGN TECHNIQUES 9**

Efficiency of Algorithms – Large Class of Recurrences – Divide and Conquer Algorithms – Dynamic Programming – Greedy Algorithms – Backtracking and Local Search Algorithms.

**UNIT IV SEARCHING AND SORTING 9**

Linear Search — Binary Search — Selection Sort — Insertion Sort — Quick Sort — Radix Sort —Merge Sort – Heap Sort – Analysis of Searching and Sorting Algorithms.

**UNIT V NP-COMPLETE PROBLEMS 9**

Nondeterministic Turing Machines – The Classes P and NP – Languages and Problems – NP Completeness of the Satisfiability Problems – Provably Intractable Problems.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES:**

At the end of the course students will be able to:

**CO1**: Understand the Principles of Algorithms and Models of Computation.

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**CO2**: Understand the Principles of Data Structures and its Applications.
**CO3**: Analyze and Design of Various Algorithms.
**CO4**: Create and Analyze Various Searching and Sorting Algorithms.
**CO5**: Understand the Principles of NP-Complete Problems.

**REFERENCES:**


1. Alfred V. Aho, John E. Hopcroft and Jeffrey D. Ullman, “The Design and Analysis of Computer Algorithms”, Pearson Education, 2017.
2. Alfred V. Aho, John E. Hopcroft and Jeffrey D. Ullman, “Data Structures andAlgorithms”, Pearson Education, 2017.
3. Udi Manber, “Introduction to Algorithms: A Creative Approach”, Addison-WesleyPublishing Company, 2017.


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**AP3058 WIRELESS SENSOR NETWORKS L T P C**

**3 0 0 3**

**UNIT I OVERVIEW OF WIRELESS SENSOR NETWORKS 9**

Challenges for Wireless Sensor Networks-Characteristics requirements-required mechanisms, Difference between mobile ad-hoc and sensor networks, Applications of sensor networks- case study, Enabling Technologies for Wireless Sensor Networks.

**UNIT II ARCHITECTURES 9**

Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes , Operating Systems and Execution Environments, Network Architecture - Sensor Network Scenarios, Optimization Goals and Figures of Merit, Gateway Concepts. Physical Layer and Transceiver Design Considerations

**UNIT III MAC AND ROUTING 9**

MAC Protocols for Wireless Sensor Networks, IEEE 802.15.4, Zigbee, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Address and Name Management, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing.

**UNIT IV INFRASTRUCTURE ESTABLISHMENT 9**

Topology Control, Clustering, Time Synchronization, Localization and Positioning, Sensor Tasking and Control.

**UNIT V DATA MANAGEMENT AND SECURITY 9**

Data management in WSN, Storage and indexing in sensor networks, Query processing in sensor,



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Data aggregation, Directed diffusion, Tiny aggregation, greedy aggregation, security in WSN, Case studies using simulation tools.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES:**

**CO1**: Ability to design implement simple wireless network concepts.
**CO2**: Ability to design, analyze implement different network architectures
**CO3**: Ability to implement MAC layer and routing protocols.
**CO4**: Ability to deal with timing and control issues in wireless sensor networks
**CO5**: Ability to analyze and design secured wireless sensor networks.

**REFERENCES**


1. Ian F. Akyildiz, Mehmet Can Vuran, “Wireless Sensor Networks”, John Wiley, January 2018.
2. Yingshu Li, My T. Thai, Weili Wu, “Wireless Sensor Networks and Applications”, Springer, 2008.
3. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless Sensor Networks", John Wiley, January 2011.
4. Feng Zhao & Leonidas J. Guibas, “Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
5. Kazem Sohraby, Daniel Minoli, & Taieb Znati, “Wireless Sensor Networks-sTechnology, Protocols, and Applications”, John Wiley, 2010.
6. Anna Hac, “Wireless Sensor Network Designs”, John Wiley, 2003.
7. Bhaskar Krishnamachari, “Networking Wireless Sensors”, Cambridge Press, 2005.
8. Mohammad Ilyas and Imad Mahgaob, “Handbook of Sensor Networks: Compact Wireless And Wired Sensing Systems”, CRC Press, 2014.
9. Wayne Tomasi, “Introduction to Data Communication and Networking”, Pearson Education, 2007.


| COs | PROGRAMME OUTCOMES | | | | | |
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**AP3007 IOT SYSTEM DESIGN AND SECURITY L T P C**
**3 0 0 3**

**UNIT I INTRODUCTION TO INTERNET OF THINGS 9**

Rise of the machines – Evolution of IoT – Web 3.0 view of IoT – Definition and characteristics of IoT – Physical design of IoT – Logical design of IoT – IoT enabling technologies – IoT levels and deployment templates – A panoramic view of IoT applications.

**UNIT II ARCHITECTURE OF IoT 9**

Identification and Access to objects and services in the IoT environment( Current technologies for



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IoT naming-Solutions proposed by research projects-Research and Future development trends and forecast) – Middleware technologies for IoT system (IoT Ecosystem Overview – Horizontal Architecture Approach for IoT Systems-SOA-based IoT Middleware)Middleware architecture of RFID,WSN,SCADA,M2M–Challenges Introduced by 5G in IoT Middleware(Technological Requirements of 5G Systems-5G-based IoT Services and Applications Requirements-5G-based Challenges for IoT Middleware) - Perspectives and a Middleware Approach Toward 5G (COMPaaS Middleware) – Resource management in IoT.

**UNIT III SECURITY CONSIDERATIONS IN IOT SMART AMBIENT SYSTEMS 9**

Security in Smart Grids and Smart Spaces for Smooth IoT Deployment in 5G (5G and the Internet of Things-Smart Spaces-Smart Grids Security and Privacy - Services that Need to Be Secure - Security Requirements -Security Attacks-Security Measures and Ongoing Research) - Security Challenges in 5G-Based IoT Middleware Systems(Security in 5G-Based IoT Middleware-Security Challenges Toward 5G).

**UNIT IV IOT ENABLERS AND THEIR SECURITY AND PRIVACY ISSUES 9**

Internet of Things layer wise Protocols and Standards- EPC global (architecture, specifications, industry adaptation, security and vulnerabilities, advantages and disadvantages)- Wireless HART-ZigBee-Near Field Communication-6LoWPAN-Dash7-Comparative Analysis.

**UNIT V APPLICATIONS AND CASE STUDIES 9**

Home automations - Smart cities – Environment – Energy – Retail – Logistics – Agriculture –Industry - Health and life style – Case study.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES:**

**At the end of the course students will be able to:**

**CO1**: Articulate the main concepts, key technologies, strength and limitations of IoT
**CO2**: Identify the architecture, infrastructure models of IoT.
**CO3**: Analyze the core issues of IoT such as security, privacy and interoperability.
**CO4**: Analyze and design different models for network dynamics.
**CO5**: Identify and design the new models for market strategic interaction.

**REFERENCES:**


1. Honbo Zhou, “Internet of Things in the cloud: A middleware perspective”, CRC press 2012.
2. Vijay Madisetti and Arshdeep Bahga, “Internet of Things (A Hands-on Approach)”, VPT, 1st Edition, 2014.
3. Constandinos X. Mavromoustakis, George Mastorakis, Jordi Mongay Batalla, “Internet of Things (IoT) in 5G Mobile Technologies” Springer International Publishing, Switzerland, 2018.
4. Dieter Uckelmann, Mark Harrison, Florian Michahelles, “Architecting the Internet of Things”, Springer-Verlag Berlin Heidelberg, 2011.
5. http://www.cse.wustl.edu/~jain/cse570-15/ftp/iot_prot/index.html.


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**AP3051 ADVANCED MICROPROCESSORS AND MICROCONTROLLERS L T P C**
**3 0 0 3**

**UNIT I MICROPROCESSOR ARCHITECTURE 9**

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.

**UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM 9**

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging — Multitasking — Exception and Interrupts — Instruction set — addressing modes – Programming the Pentium processor.

**UNIT III HIGH PERFORMANCE RISC ARCHITECTURE – ARM 9**

Organization of CPU — Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

**UNIT IV MSP430 16 - BIT MICROCONTROLLER 9**

The MSP430 Architecture- CPU Registers - Instruction Set, On-Chip Peripherals - MSP430 - Development Tools, ADC - PWM - UART - Timer Interrupts - System design using MSP430Microcontroller.

**UNIT V PIC MICROCONTROLLER 9**

CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/D Converter –PWM and introduction to C-Compilers.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES:**

**CO1**: Ability to learn the fundamentals of microprocessor architecture.
**CO2**: Ability to know and appreciate the high performance features in CISC architecture.
**CO3**: Ability to know and appreciate the high performance features in RISC architecture.
**CO4**: Ability to perceive the basic features in Motorola microcontrollers.
**CO5**: Ability to interpret and understand PIC Microcontroller.

**REFERENCES:**


1. Daniel Tabak , „" Advanced Microprocessors" McGraw Hill.Inc., 2nd Edition, November 2011.
2. James L. Antonakos , " The Pentium Microprocessor", Pearson Education , January 2002.
3. Steve Furber , " ARM System –On –Chip architecture", Addision Wesley , January 2014.
4. Gene .H.Miller ." Micro Computer Engineering ", Pearson Education , 2003.
5. John .B.Peatman , " Design with PIC Microcontroller" , Prentice hall, January 2002.
6. John H.Davis , "MSP 430 Micro controller basics", Elsevier, 2008.
7. James L.Antonakos, "An Introduction to the Intel family of Microprocessors", Pearson Education 1999, Content Revision added Date 2020.
8. Barry.B.Breg, "The Intel Microprocessors Architecture, Programming and Interfacing " , PHI,2008.




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9. Valvano "Embedded Microcomputer Systems", January 2012.
10. Readings: Web links -- www.ocw.mit.edu, www.arm.com

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| **CO5** | 1 | | 1 | 3 | 2 | 1 |

**AP3052 ELECTRONICS FOR SOLAR POWER L T P C**

**3 0 0 3**

**UNIT I INTRODUCTION TO SOLAR POWER 9**

Semiconductor – properties - energy levels - basic equations of semiconductor devices physics - Basic characteristics of sunlight - Solar angles - day length - angle of incidence on tilted surface — Sun path diagrams — Equivalent circuit of PV cell, PV cell characteristics (VI curve, PV curve) - Maximum power point, $V_{mp}$, $I_{MP}$, $V_{oc}$, $I_{SC}$ – types of PV cell - Block diagram of solar photo voltaic system, PV array sizing.

**UNIT II DC-DC CONVERTER 9**

Principles of step-down and step-up converters – Analysis and design issues of buck, boost, buck-boost and Cuk converters – time ratio and current limit control – Case Study: Solar power based power system design with converters.

**UNIT III MAXIMUM POWER POINT TRACKING 9**

Direct Energy transmission, Impedance Matching, Maximum Power Point Tracking (MPPT) - Function of MPPT, P&O method, INC Method, Fractional Open circuit voltage method, Fractional short circuit current method, parasitic capacitance and other MPPT techniques, Development of hardware, algorithms using processors for Standalone and Grid tied systems.

**UNIT IV BATTERY 9**

Types of Battery, Battery Capacity — Units of Battery Capacity-impact of charging and discharging rate on battery capacity-Columbic efficiency-Voltage Efficiency, Charging – Charge Efficiency, Charging methods, State of Charge, Charging Rates, Discharging - Depth of discharge-Discharge Methods, selection of Battery and sizing, Case study: Electric vehicle Battery Management System (EV-BMS).

**UNIT V SIMULATION OF PV MODULE & CONVERTERS 9**

Matalb Simulation of PV module - VI Plot, PV Plot, finding $V_{MP}$, $I_{MP}$, $V_{oc}$, $I_{sc}$ of PV module, Simulation of DC to DC converter -buck, boost, buck-boost and Cuk converters, standalone and grid tied photo voltaic system. FPGA based design and simulation of MPPT controllers.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES:**

**CO1**: Ability to collect solar power characteristics at a given location.

**CO2**: Ability to design and realize dc-dc converters for solar power utilization



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**CO3**: Ability to design algorithms for improving solar power utilization.
**CO4**: Ability to deal with battery issues and selection.
**CO5**: Ability to design and simulate PV systems to validate its performance.

**REFERENCES**:


1. ChetanSingh Solanki, "SolarPhotovoltaic: Fundamentals, Technologies and Applications", PHI Ltd., 3rd Edition, 2015.
2. Ned Mohan, Undeland and Robbin, "Power Electronics: converters, Application and Design", John Wiley and sons.Inc, Newyork, 3rd Edition, 2007.
3. Tommarkvart, Luis castaner, "Solar cells; materials, manufacture and operation", Elsevier, 2005.
4. G.D .Rai, "Solar energy utilization ", Khanna publishes, 1995.


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| **CO2** | 2 | 1 | 2 | 2 | 3 | 3 |
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| **CO4** | 3 | 1 | 3 | 3 | 3 | 3 |
| **CO5** | | | | 2 | 3 | 3 |

**AP3056 ROBOTICS AND INTELLIGENT SYSTEMS L T P C**

**3 0 0 3**

**UNIT I INTRODUCTION 9**

Basic Concepts such as Definition, three laws, DOF, Misunderstood devices etc., Elements of Robotic Systems i.e. Robot anatomy, Classification, Associated parameters i.e. resolution, accuracy, repeatability, dexterity, compliance, RCC device, etc. Automation-Concept, Need, Automation in Production System, Principles and Strategies of Automation, Basic Elements of an Automated System, Advanced Automation Functions, Levels of Automations, introduction to automation productivity.

**UNIT II ROBOT GRIPPERS 9**

Types of Grippers, Design aspect for gripper, Force analysis for various basic gripper system. Sensors for Robots:- Characteristics of sensing devices, Selections of sensors, Classification and applications of sensors. Types of Sensors, Need for sensors and vision system in the working and control of a robot.

**UNIT III DRIVES AND CONTROL SYSTEMS 9**

Types of Drives, Actuators and its selection while designing a robot system. Types of transmission systems, Control Systems -Types of Controllers, Introduction to closed loop control .Control Technologies in Automation:- Industrial Control Systems, Process Industries Verses Discrete-Manufacturing Industries, Continuous Verses Discrete Control, Computer Process and its Forms. Control System Components such as Sensors, Actuators and others.

**UNIT IV MACHINE VISION SYSTEM 9**

Vision System Devices, Robot Programming:- Methods of robot programming, lead through programming, motion interpolation, branching capabilities, WAIT, SIGNAL and DELAY commands,



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subroutines, Programming Languages: Introduction to various types such as RAIL and VAL II etc, Features of type and development of languages for recent robot systems.

**UNIT V MODELING AND SIMULATION FOR MANUFACTURING PLANT AUTOMATION 9**

Introduction, need for system Modeling, Building Mathematical Model of a manufacturing Plant, Modern Tools- Artificial neural networks in manufacturing automation, AI in manufacturing, Fuzzy decision and control, robots and application of robots for automation. Artificial Intelligence:- Introduction to Artificial Intelligence, AI techniques, Need and application of AI. Other Topics in Robotics:- Socio-Economic aspect of robotisation. Economical aspects for robot design, Safety for robot and associated mass, New Trends & recent updatesin robotics.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES:**

**CO1**: Ability to implement simple concepts associated with Robotics and Automation.
**CO2**: Ability to use various Robotic sub-systems.
**CO3**: Ability to use kinematics and dynamics to design exact working pattern of robots.
**CO4**: Ability to implement computer vision algorithms for robots.
**CO5**: Be aware of the associated recent updates in Robotics.

**REFERENCES:**


1. John J. Craig," Introduction to Robotics (Mechanics and Control)", Addison-Wesley, 2nd Edition, 2004.
2. Mikell P. Groover et. Al., "Industrial Robotics: Technology, Programming and Applications",McGraw – Hill International, 2nd Edition 2017.
3. Shimon Y. Nof, "Handbook of Industrial Robotics", John Wiley Co, 2001.
4. Automation, "Production Systems and Computer Integrated Manufacturing", M.P. Groover,Pearson Education, 4th Edition 2016.
5. W.P. David, "Industrial Automation", John Wiley and Sons, 1989.
6. Richard D. Klafter, Thomas A. Chemielewski, Michael Negin, "Robotic Engineering: An Integrated Approach", Prentice Hall India, 2002.
7. R.C. Dorf, "Handbook of design, manufacturing & Automation" John Wiley and Sons, 1994.


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| **CO1** | 1 | | 2 | 2 | 2 | |
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| **CO3** | 1 | | 1 | | | |
| **CO4** | 1 | | 2 | 1 | | |
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**AP3055 RF INTEGRATED CIRCUIT DESIGN L T P C**
**3 0 0 3**

**UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES 9**

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct up conversion Transmitter, Two step up conversion Transmitter.



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**UNIT II IMPEDANCE MATCHING AND AMPLIFIERS 9**

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

**UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS 9**

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model — Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

**UNIT IV MIXERS AND OSCILLATORS 9**

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

**UNIT V PLL AND FREQUENCY SYNTHESIZERS 9**

Linearized Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**:

**CO1**: Ability to explore user specifications for RF systems
**CO2**: Ability to analyze and design RF low noise amplifiers.
**CO3**: Ability to analyze and design RF power amplifiers.
**CO4**: Ability to analyze and design RF mixers and oscillators
**CO5**: Ability to design PLL for RF applications.

**REFERENCE BOOKS:**


1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 2nd Edition, January 2013.
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 1997.
4. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2nd Edition, 2017.
5. Recorded lectures and notes available at http://www.ee.iitm.ac.in/~ani/ee6240/


| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | | 3 | 1 | 2 | 2 |
| **CO2** | 3 | | 3 | 1 | 2 | 2 |
| **CO3** | 3 | | 3 | 1 | 2 | 2 |
| **CO4** | 3 | | 3 | 1 | 2 | 2 |
| **CO5** | 3 | | 3 | 1 | 2 | 2 |

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**AP3057** **SIGNAL INTEGRITY FOR HIGH SPEED DESIGN** **L T P C**
**3 0 0 3**

**UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9**

Transmission line equations, wave solution, wave *vs*. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations — L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin- effect, dispersion.

**UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9**

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far- end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossless models.

**UNIT III NON-IDEAL EFFECTS 9**

Non-ideal signal return paths — gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses — Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors.

**UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9**

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis.

**UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9**

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES:**

**CO1**: Ability to identify sources affecting the speed of digital circuits.
**CO2**: Ability to identify methods to improve the signal transmission characteristics
**CO3**: Ability to analyze non-ideal effects
**CO4**: Ability to analyze system power dissipation
**CO5**: Ability to analyze clocking strategies.

**REFERENCES**


1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice HallPTR, 1st Edition 2012.
3. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.
4. Eric Bogatin, Signal Integrity – Simplified, Prentice Hall PTR, 1st Edition 2003.


**TOOLS REQUIRED**

1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html



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2. HSPICE from synopsis, www.synopsys.com/products/ mixedsignal/hspice/hspice.html
3. SPECCTRAQUEST from Cadence, http://www.specctraquest.com

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
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| **CO1** | 2 | | 3 | | | 1 |
| **CO2** | 2 | | 3 | | 1 | |
| **CO3** | 2 | | 3 | | 1 | |
| **CO4** | 2 | | 3 | | 1 | |
| **CO5** | 2 | | 3 | | 1 | |

**AP3053 EMI AND EMC IN SYSTEM DESIGN L T P C**

**3 0 0 3**

**UNIT I EMI/EMC CONCEPTS 9**

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

**UNIT II EMI COUPLING PRINCIPLES 9**

Conducted, radiated and transient coupling; Common ground impedance coupling; Common mode and ground loop coupling; Differential mode coupling; Near field cable to cable coupling,cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

**UNIT III EMI CONTROL TECHNIQUES 9**

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

**UNIT IV EMC DESIGN OF PCBS 9**

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations

**UNIT V EMI MEASUREMENTS AND STANDARDS 9**

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES:**

**CO1**: Ability to gain knowledge to understand the concept of EMI / EMC related to product design & development.

**CO2**: Ability to analyze the different EM coupling principles and its impact on performance of electronic system.

**CO3**: Ability to analyze electromagnetic interference, highlighting the concepts of both susceptibility and immunity

**CO4**: Ability to interpret various EM compatibility issues with regard to the design of PCBs and ways toimprove the overall system performance

**CO5**: Ability to obtain broad knowledge of various EM radiation measurement techniques and the present leading edge industry standards in different countries



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**REFERENCES:**


1. V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press,Newyork, 1996.
2. Henry W.Ott.,”Noise Reduction Techniques in Electronic Systems”, A Wiley Inter SciencePublications, John Wiley and Sons, Newyork, 1988.
3. Bemhard Keiser, “Principles of Electromagnetic Compatibility”, Artech house, Norwood, 3rdEdition, 3rd Edition 1987.
4. C.R.Paul,”Introduction to Electromagnetic Compatibility”, John Wiley and Sons, Inc, 2nd Edition 2010.
5. Don R.J.White Consultant Incorporate, “Handbook of EMI/EMC”, Vol I-V, 1988.


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| **CO1** | | | 2 | | | |
| **CO2** | 1 | | | | 3 | 3 |
| **CO3** | | | 2 | | | |
| **CO4** | | | 2 | 3 | 2 | 3 |
| **CO5** | | | | | 3 | 2 |
| **CO6** | | | | 3 | 1 | |

**AP3008 ARTIFICIAL INTELLIGENCE AND OPTIMIZATION TECHNIQUES L T P C**
**3 0 0 3**

**UNIT I NEURAL NETWORKS 9**

Neural Networks: Back Propagation Network, generalized delta rule, Radial Basis Function Network, interpolation and approximation RBFNS, comparison between RBFN and BPN, Support Vector Machines: Optimal hyperplane for linearly separable patterns, optimal hyperplane for nonlinearly separable patterns, Inverse Modeling.

**UNIT II FUZZY LOGIC SYSTEMS 9**

Fuzzy Logic System: Basic of fuzzy logic theory , crisp and fuzzy sets, Basic set operation like union , interaction , complement , T-norm , T-conorm , composition of fuzzy relations, fuzzy if- then rules , fuzzy reasoning, Neuro-Fuzzy Modeling: Adaptive Neuro-Fuzzy Inference System (ANFIS) , ANFIS architecture , Hybrid Learning Algorithm.

**UNIT III EVOLUTIONARY COMPUTATION & GENETIC ALGORITHMS 9**

Evolutionary Computation (EC) — Features of EC — Classification of EC — Advantages — Applications. Genetic Algorithms: Introduction – Biological Background – Operators in GA-GA Algorithm – Classification of GA – Applications

**UNIT IV ANT COLONY OPTIMIZATION 9**

Ant Colony Optimization: Introduction – From real to artificial ants- Theoretical considerations – Convergence proofs – ACO Algorithm – ACO and model based search – Application principles of ACO.

**UNIT V PARTICLE SWARM OPTIMIZATION 9**

Particle Swarm Optimization: Introduction – Principles of bird flocking and fish schooling – Evolution of PSO – Operating principles – PSO Algorithm – Neighborhood Topologies –



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Convergence criteria – Applications of PSO, Honey Bee Social Foraging Algorithms, Bacterial Foraging Optimization Algorithm.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES:**

**CO1**: Ability to design and train neural networks with different rules..
**CO2**: Ability to devise fuzzy logic rules.
**CO3**: Ability to implement genetic algorithms.
**CO4**: Ability to implement ANT colony optimization technique for various problems.
**CO5**: Ability to use PSO technique.

**REFERENCES:**


1. Wolfgang Ertel, “Introduction to Artificial Intelligence”, Springer, 2 Edition, 2017
2. Nello Cristianini, John Shawe-Taylor, "An Introduction to Support Vector Machines and Other Kernel-based Learning Methods”, Cambridge University Press. 2013
3. Christopher M. Bishop, “Neural Networks for Pattern Recognition”, Oxford University Press,1995
4. H.-J. Zimmermann, “Fuzzy Set Theory and its Applications”, Springer Science+BusinessMedia New York, 4th edition, 2001
5. David E. Goldberg, “Genetic Algorithms in search, Optimization & Machine Learning”, Pearson Education, 2006
6. Kenneth A DeJong, “Evolutionary Computation A Unified Approach”, Prentice Hall of India,New Delhi, 2006.
7. Marco Dorigo and Thomas Stutzle, “Ant Colony optimization”, Prentice Hall of India, NewDelhi, 2004.
8. N P Padhy, “Artificial Intelligence and Intelligent Systems”, Oxford University Press, 2005.
9. Engelbrecht, A.P., “Fundamentals of Computational Swarm Intelligence”, Wiley, 2005.


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| **CO1** | | | 2 | 2 | | |
| **CO2** | | | 3 | 2 | | |
| **CO3** | 1 | | 3 | 3 | | |
| **CO4** | 1 | | 3 | 2 | 1 | 1 |
| **CO5** | | | 3 | 3 | | |

PROGRESS THROUGH KNOWLEDGE

**AP3009 NANOELECTRONICS L T P C**
**3 0 0 3**

**UNIT I INTRODUCTION TO NANO ELECTRONICS 9**

Scaling to nano-Light as a wave and particle- Electrons as waves and particles- origin of quantum mechanics-General postulates of quantum mechanics-Spin and angular momentum-Wave packets and uncertainty.

**UNIT II ELECTRONS CONFINEMENT IN LOW DIMENSIONAL STRUCTURES 9**

Statistics of the electrons in solids and nanostructures, Density of states in nanostructures, Time independent Schrodinger wave equation- Electron confinement-Quantum dots, electron



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confinement Quantum wires, electron confinement Quantum wells.

**UNIT III GROWTH, FABRICATION AND MEASUREMENT TECHNIQUES FOR NANOSTRUCTURES 9**

Bulk crystal and heterostructure growth, Nanolithography, etching, and other means for fabrication of nanostructures and nanodevices, Techniques for characterization of nanostructures (SEM, AFM,TEM), Spontaneous formation and ordering of nanostructures, Clusters and nanocrystals Methods of nanotube growth, Chemical and biological methods for nanoscale fabrication, Fabrication of nano electro mechanical systems.

**UNIT IV NANOELECTRONICS DEVICES 9**

Coulomb blockade- Single electron transistors, Semiconductor nanowire SETs, Field-effect transistors, Quantum Cellular automata, Light emitting diodes and lasers, Carbon nanotube transistors, Semiconductor nanowire FETs and SETs, Molecular SETs and Molecular Electronics.

**UNIT V TUNNEL JUNCTIONS AND APPLICATIONS OF TUNNELING 9**

Tunnelling through a potential barrier, Potential energy profiles in material interfaces, Applications of tunnelling, Field emissions, Gate oxide Tunnelling and Hot electron effects in MOSFETS, Scanning tunnelling microscope, Double barrier tunnelling and Resonant tunnelling diode

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**:

**CO1**: Ability to familiarise the fundamental underpinnings of nano electronics.
**CO2**: Ability to analyse the electron properties of traditional low dimensional structures.
**CO3**: Analyse the growth, fabrication and measurement techniques of nanostructured devices.
**CO4**: Ability to analyse the key performance of nano electronic devices.
**CO5**: Ability to explore the basics of tunnelling devices.

**REFERENCES:**


1. Hanson, “Fundamentals of Nanoelectronics”, Pearson education, 2009.
2. V. Mitin, V. Kochelap, and M. Stroscio, Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications, Cambridge University Press, 2008.
3. Jan Dienstuhl, Karl Goser, and Peter Glösekötter, “Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices”, Springer-Verlag, 2004. (Unit II, IV & V)
4. Mircea Dragoman, Daniela Dragoman, Nanoelectronics: Principles and Devices, Artech House, 2009.
5. Robert Puers, Livio Baldi, Marcel Van de Voorde, Sebastiaan E. van Nooten, Nanoelectronics: Materials, Devices, Applications, Wiley, 2017.


| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
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| **CO1** | | | 2 | 2 | | |
| **CO2** | | | 3 | 2 | | |
| **CO3** | 1 | | 3 | 3 | | |
| **CO4** | 1 | | 3 | 2 | 1 | 1 |
| **CO5** | | | 3 | 3 | | |



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**VL3054** **MEMS AND NEMS** **L T P C**
**3 0 0 3**

**UNIT I INTRODUCTION AND FABRICATION OF MEMS 9**

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Microaccelorometers and Micro fluidics, Materials for MEMS: Silicon, silicon compounds, polymers, metals. Photolithography, Ion Implantation, Diffusion, Oxidation, Dry and wet etching, Bulk Micromachining, Surface Micromachining, LIGA

**UNIT II INTRODUCTION AND FABRICATION OF NEMS 9**

Introduction to NEMS, Nano scaling, classification of nano structured materials, Applications of nanomaterials. Synthesis routes – Bottom up and Top down approaches.
Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation

**UNIT III DESIGN OF MEMS SENSORS AND ACTUATORS 9**

Acoustic sensor – Quartz crystal microbalance, Surface acoustic wave, Flexural plate wave, shear horizontal; Vibratory gyroscope, Pressure sensors, Electrostatic actuators, piezoelectric actuators, Thermal actuators, Actuators using shape memory alloys, Microgrippers, Micromotors, Microvalves, Micropumps.

**UNIT IV NEMS MATERIALS AND SENSORS 9**

Quantum dots, Carbon nanotubes, Nanocrystalline ZnO, Nanocrystalline Titanium Oxide, Multilayered Films, Quantum well infrared photodetectors.

**UNIT V INTRODUCTION TO OPTICAL AND RF MEMS 9**

Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF MEMS – design basics, case study – Capacitive RF MEMS switch, performance issues.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**:

**At the end of the course student will be able to:**

**CO1**:Recognize the basics of materials and fabrication of micro electromechanical systems.
**CO2**:Devise the fabrication techniques of nano electromechanical systems
**CO3**:Analyze the key performance aspects of micro electromechanical sensors and transducers.
**CO4**:Analyze various aspects of nano materials and sensors.
**CO5**:Identify the potential applications of MEMS in the RF and optical domain

**REFERENCES:**


1. Ran Hsu, MEMS and Microsystems Design and Manufacture, Tata Mcgraw Hill, 2002.
2. Murty B.S, Shankar P, Raj B, Rath, B.B, Murday J, Textbook of Nanoscience and Nanotechnology, Springer publishing, 2013
3. Sergey Edward Lyshevski, “MEMS and NEMS: Systems, Devices, and Structures”, CRC Press, 2002
4. Chang Liu, “Foundations of MEMS”, Pearson education India limited, 2006.
5. Vinod Kumar Khanna Nanosensors: Physical, Chemical, and Biological, CRC press, 2012.
6. Mahalik N P, MEMS, Tata McGraw Hill, 2007.
7. Manouchehr E Motamedi, MOEMS: Micro-Opto-Electro-Mechanical Systems, SPIE




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press, First Edition, 2005.

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|---|---|---|---|---|---|---|
| **CO1** | | | 2 | 2 | | |
| **CO2** | | | 3 | 2 | | |
| **CO3** | 1 | | 3 | 3 | | |
| **CO4** | 1 | | 3 | 2 | 1 | 1 |
| **CO5** | | | 3 | 3 | | |

**VL3052 FUNDAMENTALS OF SPINTRONICS AND QUANTUM COMPUTING L T P C**
**3 0 0 3**

**UNIT I LAWS OF SPINTRONICS AND SPIN ORBIT 9**

The Early History of Spin, Quantum Mechanics of Spin, Spin – Orbit interaction, Spin – Orbit interaction of Solids.

**UNIT II SPIN ELETRON TRANSPORT 9**

Basic Electron Transport, Basic Electron Transport in thin film, Conduction in Discontinuous film, Magneto-resistance, Spin-Dependent Scattering, Giant Magneto Resistance, Spin Dependent Tunneling, Tunnel Magnetoresistance, MTJ, STT, SOT.

**UNIT III SPIN TRANSISTOR 9**

Silicon based spin electron device, Spin field effect transistor Spin injection, spin diffusion, Spin LED: Fundamental and Application, Spin photo electronics Devices

**UNIT IV ELECTRON SPINS IN QUANTUM DOTS AS QUBITS 9**

Conventional Vs Quantum Computing - Quantum Communication - Requirements for Quantum Computing - Coupled Quantum Dots as Quantum Gates - Single-Spin Rotations - Read-Out of a Single Spin.

**UNIT V QUANTUM COMPUTING WITH SPINS 9**

The quantum inverter - NAND without energy dissipation - Universal reversible gate: Toffoli-Fredkin gate, A-matrix – Quantum gate, Superposition states – Quantum parallelism - Universal quantum gates.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**:

At the end of this course students will be able to

**CO1**: Ability to learn the laws of spintronics and spin orbit.
**CO2**: Ability to obtain spin based transport and its characteristics.
**CO3**: Identify the types of spintronics based devices.
**CO4**: Design quantum gates using qubits.
**CO5**: Apply the quantum principles to quantum universal gates.

**REFERENCES:**


1. Bandyopadhyay S, Cahay M. Introduction to spintronics. CRC press; 2015.
2. Awschalom DD, Loss D, Samarth N, editors. Semiconductor spintronics and quantum computation. Springer Science & Business Media; 2013.




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3. Hedin ER, Joe YS, editors. Spintronics in nanoscale devices. CRC Press; 2013 Aug 20.
4. D. J. Sellmyer, R. Skomski. Advanced Magnetic Nanostructures. Springer Publishers, 2005.
5. S. Maekawa. Concepts in Spin Electronics. Oxford University Press; 2006.
6. D.D. Awschalom, R.A. Buhrman, J.M. Daughton, S.V. Molnar, and M.L. Roukes, Spin Electronics, Kluwer Academic Publishers, 2004.
7. Y.B. Xu and S.M.Thompson. Spin Materials and Technology. Taylor & Francis, 2006.

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | | 3 | 2 | 1 | |
| **CO2** | 3 | | 3 | 3 | 1 | |
| **CO3** | 3 | | 3 | 3 | 1 | |
| **CO4** | 3 | | 3 | 3 | 1 | |
| **CO5** | 3 | | 3 | 3 | 1 | |

**AP3010 SYSTEM DESIGN USING HARDWARE DESCRIPTION LANGUAGES L T P C**

**2 0 2 3**

**UNIT I BASICS OF VHDL 6**

Entity declaration - Architecture body - Creating I/O Ports for Different Data Types – Signal, Constant and variable - VHDL operators - Assignment operators, Logical operators, arithmetic operators and shift operators – Generic statement – VHDL statements - concurrent signal assignment statements and sequential statements – Packages, Components, Functions and Procedures – Test bench.

**UNIT II BASICS OF VERILOG 6**

Module – Module ports - Verilog operators – Data types – net, reg declarations - Constants and Arrays – Module parameters - Continuous and Procedural Assign statements – Conditional Expressions – Sequential statements - blocking and non-blocking assignments - Primitive instantiations – Module instantiations – Compiler directives – Test bench.

**UNIT III SYSTEM DESIGN WITH VHDL AND VERILOG 6**

Combinational Circuit Design – Adder, Subtractor, Comparator, Priority encoder, Mux/Demux, Code converters, Array multiplier – Sequential circuit design – Latch, Flip flops, Registers, Shift registers, Counters, Sequential multiplier, State machine designs.

**UNIT IV DESIGN CONSIDERATIONS VERIFICATION 6**

Timing Parameters – Metastability – Positive and Negative Clock skew – Setup slack and Hold slack – Clock latency – Area, Speed and Power requirements, Testing and verification.

**UNIT V CASE STUDIES 6**

A Pipelined Multiplier Accumulator – ALU Design – Single port and Dual port Memory design – Design of ALU, DSP modules and MAC unit.



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**LAB EXPERIMENTS:**

1. Implementation of Logic gates
2. Implementation of Mux and Demux
3. Implementation of Encode and Decoder
4. Implementation of Adders and Subtractors
5. Implementation of Flip-flops
6. Implementation of Counters
7. Implementation of registers
8. Implementation of simple state machine

**TOTAL: 30+30 = 60 PERIODS**

**COURSE OUTCOMES:**

**At the end of this course students will be able to:**

**CO1**: Understand the basic data types and operators of Verilog
**CO2**: Understand the basic data types and operators of VHDL
**CO3**: Design arithmetic modules using Verilog and VHDL
**CO4**: Analyse power dissipation and propagation delay of the RTL modules
**CO5**: Design macro modules such as ALU, MAC etc

**REFERENCES:**


1. Pong P.Chu, RTL Hardware Design using VHDL Coding for Efficiency, Portability, and Scalability, Wiley Interscience Publication, 2006, ISBN-13:978-0-471-72092-8
2. Ming Bo Lin, Digital System Designs and Practices – using Verilog HDL and FPGAs, Wiley India Pvt. Ltd., 2008, Reprint 2012.
3. Peter J.Ashenden, The Designer's Guide to VHDL, Third Edition, Elsevier, 2008. ISBN: 978-0-12-088785-9.
4. Peter J.Ashenden, Digital Design – An Embedded Systems Approach using Verilog, Elsevier Inc., 2008, ISBN: 978-0-12-369527-7.
5. Vaibbhav Taraate, ASIC Design and Synthesis – RTL Design using Verilog, Springer, 2021.


| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
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| **CO1** | 1 | | | 2 | 1 | |
| **CO2** | 2 | 2 | 3 | 2 | 1 | |
| **CO3** | 1 | | | 2 | 1 | |
| **CO4** | 3 | 3 | 3 | 3 | 1 | |
| **CO5** | | | | 2 | 1 | |

**VL3055 NEUROMORPHIC COMPUTING L T P C**
**3 0 0 3**

**UNIT I INTRODUCTION TO NEUROMORPHIC ENGINEERING 9**

Introduction to neuromorphic engineering, Non-von Neumann computing approach, Neuron, Synapse, Synaptic plasticity rules, spike-time-dependent plasticity, Signaling and operation of Biological neurons, Neuron models- LIF, IF, HH.

**UNIT II SENSORY SYSTEMS AND LEARNING 9**

Silicon retina, silicon cochlea, electronic nose, learning in silicon – supervised and unsupervised



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learning, Hebbian learning in silicon and cognitive functions in silicon – recognition, attention, artificial consciousness, Hybrid Neuron-Silicon system - Hodgkin-Huxley Model , Volterra-Poisson Model.

**UNIT III NEUROMORPHIC COMPUTING 9**

Spiking Neural Networks, Advanced Nanodevices for Neuron Implementation, Synaptic emulation - non-volatile memory, Flash, RRAM, Electro-chemical RAM, memristors, CNT, Interconnection Networks; Interconnection schemes for large non-spiking and spiking neural networks.

**UNIT IV NEUROMORPHIC HARDWARE IMPLEMENTATION 9**

Hardware Implementation: Electronic synapses, Hardware Implementation of Neuron circuits, Hardware Implementation of Synaptic and Learning circuits, and System Design: Analysis of digital neuromorphic system design, architecture and performance characteristics of demonstrated chips employing digital neuromorphic VLSI, electronic synapses and other neuromorphic systems.

**UNIT V NETWORK DESIGN 9**

Network Design, Network design example for visual application, auditory application, full system level power/energy dissipation considerations.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**:

**CO1**: Ability to learn how electronics circuits mimic biological neurons.
**CO2**: Ability to implement learning techniques and cognitive functions in Silicon.
**CO3**: Ability to build power-saving hardware building blocks for neuromorphic systems.
**CO4**: Ability to design and develop neuromorphic circuits.
**CO5**: Ability to implement commercial neuromorphic system design for various real-world applications.

**REFERENCES:**


1. Eric Kandel, James Schwartz, Thomas Jessell, Steven Siegelbaum, A.J. Hudspeth, Principles of neural science, McGraw Hill 2012, ISBN 0071390111
2. Dale Purves, Neuroscience, Sinauer, 2008, ISBN 0878936971
3. Shih-Chii Liu, Jörg Kramer, Giacomo Indiveri, Tobias Delbrück, Rodney Douglas, Analog VLSI: circuits and principles, MIT press, 2002, ISBN 0262122553
4. Carver Mead, Analog VLSI and neural systems, Addison-Wesley, 1989, ISBN0201059924
5. Kozma, R., (2012), Advances in Neuromorphic Memristor Science, Springer
6. Review papers on Neuromorphic Computing.


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| **CO1** | 2 | | 3 | 3 | 2 | |
| **CO2** | 2 | | 3 | 3 | 2 | |
| **CO3** | 2 | | 3 | 3 | 2 | |
| **CO4** | 2 | | 3 | 3 | 2 | |
| **CO5** | 2 | | 3 | 3 | 2 | |

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| VL3053 | MACHINE LEARNING IN VLSI DESIGN | L T P C<br>3 0 0 3 |
|---|---|---|

**UNIT I INTRODUCTION TO MACHINE LEARNING ARCHITECTURE 9**

Artificial Neural Networks – Artificial Neuron and its mathematical model, Activation functions, Biases and threshold, Linear separability, Neural network architecture: single layer and multilayer feed forward networks, Learning Paradigms-Supervised, Unsupervised and reinforcement Learning, Architecture for Multiply and Accumulate unit, Special function unit for Sigmoid and ReLu activation functions.

**UNIT II SUPERVISED LEARNING AND UNSUPERVISED LEARNING 9**

Multilayer Perceptron - Back propagation learning algorithm, Radial-basis function Networks Kernels and Support vector machines, Unsupervised learning - K Nearest Neighbors, Self-organizing Feature Maps, Gaussian Mixture Models.

**UNIT III DEEP NEURAL NETWORKS 9**

Convolutional Neural basics: kernels, padding, stride, channels, activation maps, Convolutional neural network: pooling, receptive field, batch normalization, Standard CNN architectures: LeNet, AlexNet, VGG, Inception, ResNet, GoogleNet, DenseNet; Performance comparison of different CNN architectures.

**UNIT IV VLSI IMPLEMENTATION OF NEURAL NETWORKS 9**

Processing element model, PE row, PE array design, Processing element tile design, Direct, FFT-based, Winograd-based, Matrix multiplication based convolutional strategies, architectures for low-energy support vector machines.

**UNIT V VLSI ARCHITECTURE FOR DEEP NEURAL NETWORKS 9**

VLSI architecture for deep neutral networks, data and instruction flow in 2D systolic array architecture, Processing optimization in 2D systolic array, Pruning, compression , Hardware Accelerator.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**:

**CO1**: Ability to build hardware blocks for neurons model
**CO2**: Ability to implement machine learning techniques
**CO3**: Ability to analyze digital implementations of Neural Network
**CO4**: Ability to implement deep neural networks
**CO5**: Ability to design energy-efficient machine learning hardware for deep neural network models.

**REFERENCES:**


1. Bishop, C. (2006). Pattern Recognition and Machine Learning. Berlin: Springer-Verilog.
2. Ethem Alpaydin, Introduction to Machine Learning, PHI
3. Jose G. Delgado-Frias, William R. Moore, “VLSI For Artificial Intelligence And Neural Networks”, Springer Science Business Media, LLC, 2001.
4. Mohamed I. Elmasry, “VLSI Artificial Neural Networks Engineering”, Springer Science Business Media, LLC, 2000.
5. Sied Mehdi Fakhraie, Kenneth C. Smith, “VLSI - Compatible Implementations for Artificial Neural Networks”, Springer Science Business Media, LLC, 1996
6. Elfadel, Ibrahim M., Duane S. Boning, and Xin Li, eds. Machine Learning in VLSI Computer-Aided Design. Springer, 2019. VLS 5234: Physical D




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| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 2 | | 3 | 3 | 1 | |
| **CO2** | 2 | | 3 | 3 | 1 | |
| **CO3** | 2 | | 3 | 3 | 1 | |
| **CO4** | 2 | | 3 | 3 | | |
| **CO5** | 2 | | 3 | 3 | | |




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